Readout circuits for multi-channel photomultiplier arrays

Executive summary
A readout circuit for multi-channel photomultiplier arrays, such as Silicon Photomultiplier (SiPM) arrays, has been developed by researchers from University of Barcelona and CIEMAT. A novel current mode input stage displaying high dynamic range and allowing operating SiPMs at high overvoltage is proposed. Together with low series noise and high bandwidth, it allows achieving excellent time resolution, compatible with Time of Flight (ToF) measurements. Furthermore, linearized Time over Threshold (ToT) energy outputs allows direct interface with programmable logic, which is optimal for low cost and reconfigurable systems. Its applications include radiation detectors, medical imaging, and optical communications.

Introduction
Most typical monolithic SiPM arrays are common cathode arrays (anode readout). However, usual current mode circuits, based on npn bipolar or nMOS common base/gate transistors, are not well suited for anode readout. In order to achieve good time resolution, SiPMs are operated at high overvoltage, and this requires high dynamic range. Also, it is important that the voltage of each input (anode) can be controlled to be able to equalize array performances. Combining these features with a flexible and inexpensive readout would be highly desirable. Additionally, considering the degradation of current PET scanners performance due to pile-up, there is a need for circuits providing means for its detection.

Description
The present integrated circuit meets all these needs. Each of its 16 channels can be connected to a SiPM array anode. A novel current mode input stage is proposed, displaying high dynamic range (up to 20 mA peak current) and allowing operating SiPMs at high overvoltage. The control of each SiPM channel overvoltage allows a higher gain and PDE uniformity. The input stage achieves low series noise, high bandwidth, high dynamic range, and low input impedance.

Combining these characteristics it is possible to achieve excellent time resolution, compatible with ToF techniques. A timing output with time resolution below 30 ps rms is generated from the fast-OR of all the channels. The energy signal (pulse charge) of each channel is encoded following a ToT scheme. Since each can be directly interfaced to a digital TDC in order to perform digitization, an ADC is not required, thus allowing the readout to be performed by a flexible and inexpensive device such a FPGA. A pile-up signal per channel flags pile-up events.

Advantages
- Optimized for SiPM array readout & high overvoltage operation:
  - No extra component
  - On-chip voltage control per channel
- Novel input stage: high dynamic range, low noise, high speed and low input impedance
  - Time resolution < 30 ps rms (ToF)
- Linearized ToT outputs: direct FPGA interface
- Pile-up detection system

Current stage of development
A prototype has been designed and built for TOF-PET and scientific applications.

Goal
Partners are sought to further develop the technology through a co-development and license agreement.

Intellectual Property
European Patent Application (December 2012)

Reference AVCRI190

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